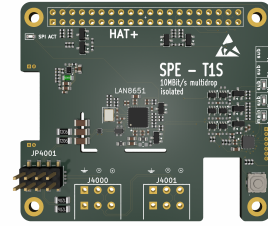


# 10BaseT1S Industrial HAT

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**10BASE-T1S (IEEE 802.3cg) enables 10 Mbit/s Ethernet communication over a single twisted pair in multidrop topologies, supporting at least 8 nodes over distances of up to at least 25 m.**

**This HAT enables multidrop communication based on 10BASE-T1S Ethernet with an onboard MAC-PHY.**

## Key Features

- 10BASE-T1S compliant with IEEE 802.3cg
- LAN8651 10BASE-T1S MAC-PHY
- Galvanically isolated MDI
- Raspberry Pi HAT+ compliant (2024)
- Stackable HAT (BE-IIS-HAT++)
- Configurable CS and IRQ routing
- Optional PoSPE support
- Two connector options available
- RoHS compliant
- Quality component suppliers

## Product Description

The 10BASE-T1S Industrial Ethernet HAT is a Raspberry Pi HAT+ compliant Single Pair Ethernet interface board in accordance with IEEE 802.3cg. It integrates a LAN8651 10BASE-T1S MAC-PHY and provides galvanic isolation between the logic side and the field-side interface.

## Applications

- Technology evaluation
- Industrial network evaluation
- Prototyping
- Education and laboratory use
- Switch and node evaluation

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## 1 Introduction

The BE-IIS HAT++ 10BASE-T1S Industrial HAT is a Raspberry Pi HAT+ compliant interface board for 10BASE-T1S communication in industrial and laboratory environments.

The board integrates a LAN8651 10BASE-T1S MAC-PHY [1]. The MDI is galvanically isolated from the logic domain.

The HAT supports multidrop 10BASE-T1S operation and can be used for evaluation, prototyping, industrial network testing, and educational purposes.

PLCA and CSMA/CD are supported and can be configured using standard Linux tools. Optionally, an add-on HAT is available to provide Power over Single Pair Ethernet (PoSPE).

The HAT is fully compatible with the Raspberry Pi Foundation HAT+ specification as well as the BE-IIS HAT++ system for advanced functionality such as stacking.

## 2 Hardware Configuration

### 2.1 Main Features

The BE-IIS-HAT++T1S enables 10BASE-T1S communication on Raspberry Pi platforms. It allows a standard Raspberry Pi platform (e.g. Raspberry Pi Zero or Raspberry Pi 3/4/5, excluding Compute Module variants) to operate as a 10BASE-T1S node. Communication between the Raspberry Pi and the onboard MAC-PHY is implemented via the SPI interface with an interrupt line for event handling.

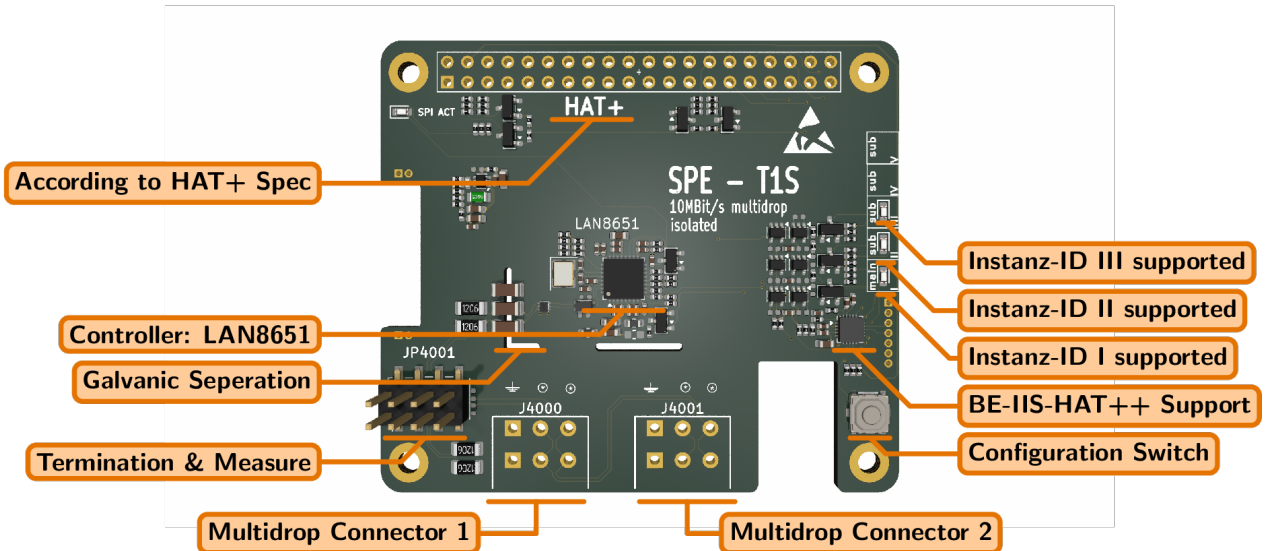


Figure 1: BE-IIS 10BASE-T1S top view with annotations

#### MAC-PHY

- Supplier: Microchip
- LAN8651 10BASE-T1S MAC-PHY
- Crystal 25MHz

#### SPI Interface

- SPI0.0, SPI0.1, and SPI0.2 supported
- Persistent selection via push button

#### Isolation

- Galvanically separated MDI
- Implemented by capacitive coupling

#### Power over Dateline

- Combination with a PoSPE HAT possible
- Supports currents up to 1 A
- Supports input voltages from 9 V to 33 V
- Includes an integrated 5 V main supply

#### Protocol Support

- 10BASE-T1S according to IEEE 802.3cg
- CSMA operation support
- PLCA operation support

#### Bus Topology

- Multidrop single-pair Ethernet architecture
- Up to 8 nodes compliant with IEEE 802.3cg
- Higher node counts depending on system design

#### Node Configuration

- Configuration via `ethtool`
- Leader node support
- Follower node support

## 2.2 Block Diagram

The block diagram shown in Figure 2 is simplified. It illustrates the main functional blocks, power domains, isolation barriers, and the principal data paths of the system.

The interrupt signal routing is not shown. It is configured using the same scheme as the chip-select (CS) routing. Reset and auxiliary control signals are omitted for clarity.

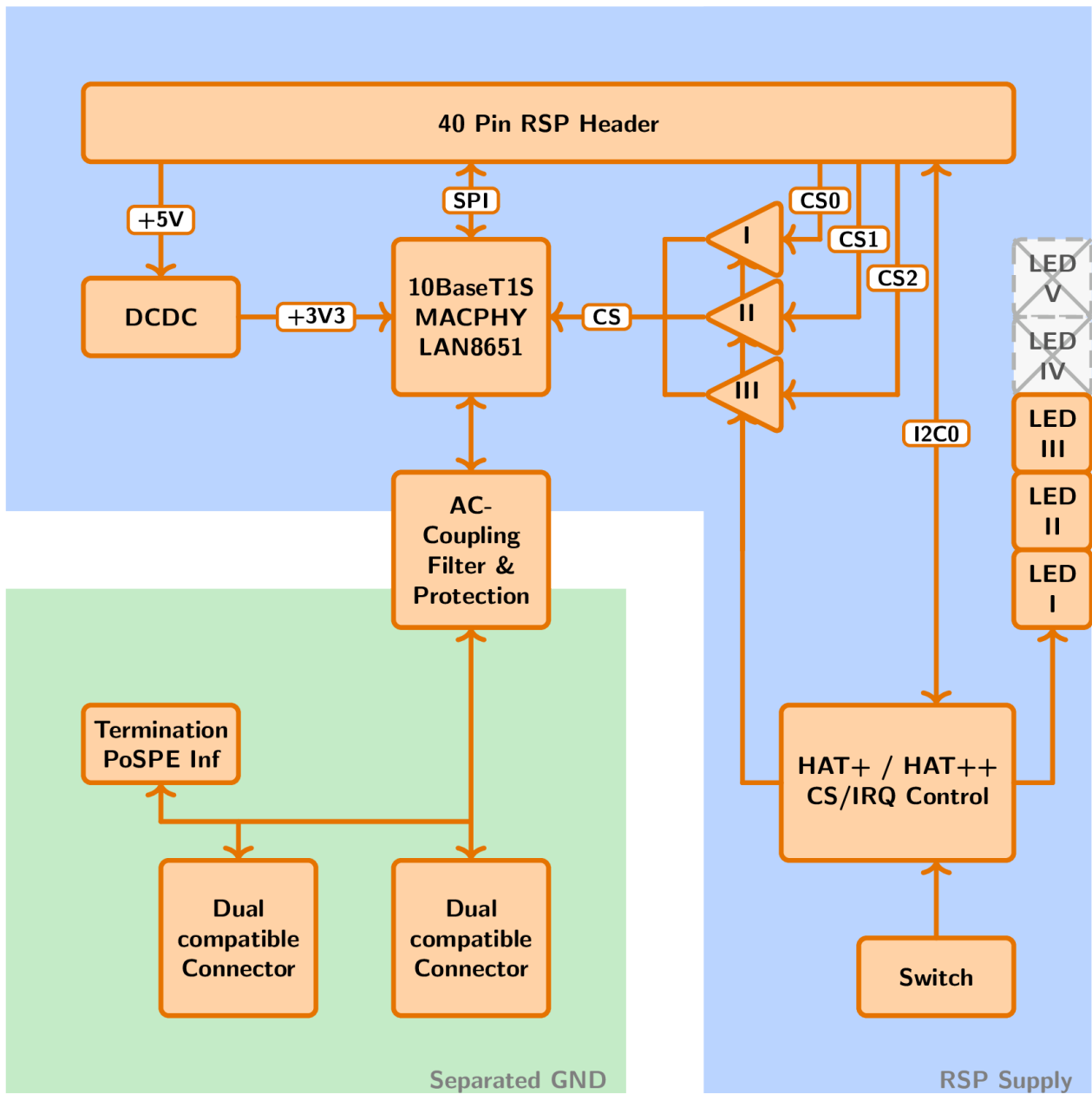


Figure 2: Simplified block diagram

## 2.3 Interfaces

The board interfaces with the host system via an SPI bus and a dedicated interrupt (IRQ) signal.

The SPI bus is used for communication between the Raspberry Pi (SPI master) and the onboard MAC-PHY (SPI slave). An interrupt line is used for event-driven communication.

The supported instance modes define the assignment of chip-select (CS) and interrupt (IRQ) signals:

Instance Mode	CS	IRQ
I	GPIO8	GPIO6
II	GPIO7	GPIO5
III	GPIO16	GPIO12

Table 1: Exclusive HW resources

Instance Mode	Signal	Pin
I & II & III	SCLK	GP11
I & II & III	MISO	GP9
I & II & III	MOSI	GP10
I & II & III	RESET	GP13
I & II & III	SCL0	GP1
I & II & III	SDA0	GP0

Table 2: Shared HW resources

The CS and IRQ signals are exclusively occupied by the HAT in each instance mode.

The SPI bus signals are shared across all instance modes. These signals may also be shared with additional HATs, provided that proper chip-select separation is ensured.

### HAT+ / HAT++ functionality

The I<sup>2</sup>C bus **I2C0** (SDA0 / SCL0) is reserved for HAT identification and configuration purposes.

An onboard controller connected to I2C0 provides standard HAT+ identification data as well as extended HAT++ metadata. This includes, for example, device tree overlay references and configuration parameters used for automatic system integration.

The EEPROM content can be evaluated by the bootloader or by user-space software to dynamically apply device tree overlays and configure the system.

All other GPIO signals remain available for user applications, unless otherwise specified.

## 2.4 Isolation

Galvanic separation is implemented between the MDI signaling domain and the Raspberry Pi domain.

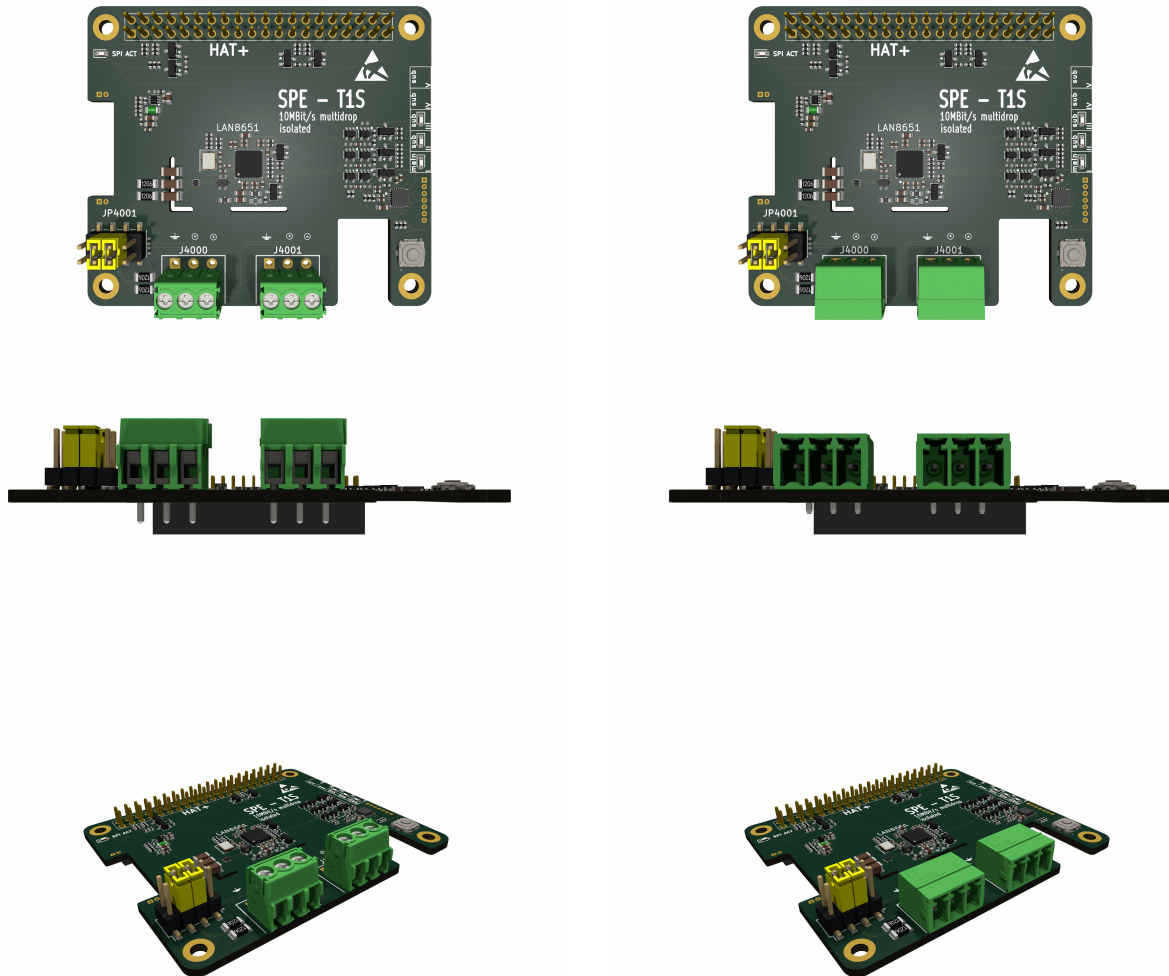
The separation barrier isolates the field-side interface from the logic-side circuitry, improving robustness against ground potential differences.

The separation is implemented by AC coupling in the MDI path using capacitors.

The isolation performance has not been formally validated. Users must evaluate the suitability of the separation concept for their specific application. Use of the isolation feature is at the user's own responsibility.

## 2.5 Connectors

Connectors J4000 and J4001 provides the physical MDI Bus interface. Both Connectors are placed on the same BUS for ease Multipdrop usage. Two commonly used connector options can be populated. on both connector lands



**Supplier:** Phoenix Contact

**MPN:** PT 1,5/3-3,5-H

**Order Code:** 1984620 [3]

**Description:** 3-pin 3.5 mm screw terminal block

**Note:** This connector is included in the delivery

**Supplier:** Phoenix Contact

**MPN:** MC 1,5/ 3-G-3,5 - PCB header

**Order Code:** 1844223 [4]

**Description:** 3-pin 3.5mm mm PCB header

## 2.6 Jumper and Configuration

Jumper JP4001 configures the bus termination for 10BASE-T1S operation.

For proper 10BASE-T1S multidrop operation, termination shall only be enabled at the two physical end nodes of the bus segment.

**End nodes:** Jumper installed (termination enabled)

**Intermediate nodes:** Jumper not installed (termination disabled)

In **point-to-point operation**, both connected devices are considered end nodes. Therefore, termination shall be enabled on both nodes.

Figure 3 shows the jumper configuration.

Pin	Signal	Pin	Signal
1	Shield	2	Shield
3	Termination	4	SPE1
5	Termination	6	SPE2
7	Shield	8	Shield

Table 3: JP4001 pin assignment

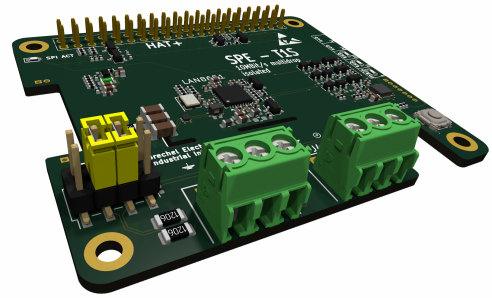


Figure 3: JP4001 termination jumper configuration with termination enabled

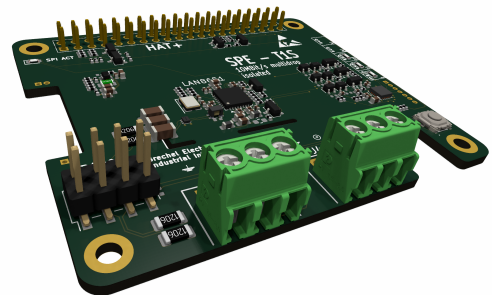


Figure 4: JP4001 termination jumper configuration with termination disabled

## 2.7 Indicators (LEDs)

In addition to the LED status bar on the side, which indicates the selected instance mode, there is one additional LED on the HAT.

- **SPI ACT:** Indicates SPI communication with the MAC-PHY

## 2.8 Signal Polarity and Wiring Orientation

The two signal wires of the 10BASE-T1S interface are not polarity-sensitive. Either wire may be connected to either signal terminal.

Both wiring orientations are valid and supported by the interface.

This applies to normal data communication as well as to operation with power over the data line [TODO].

## 3 Software and System Configuration

The BE-IIS-HAT++ system provides a unified platform for fast system integration.

- Predefined drivers and kernel modules

- Support for prebuilt modules and custom kernel builds
- Ready-to-use build and configuration scripts
- Centralized software repository (see Reference 2)
- Typical setup time below a few minutes

After installation, the system can be used without further software modification.

## 4 Electrical Specifications

### 4.1 Supply Voltage

Parameter	Min	Typ	Max
3.3 V Input [V]	3.135	3.3	3.65
5 V Input [V]	4.5	5	5.5

Table 4: Voltage supply

### 4.2 Power Consumption

Parameter	Typ	Unit
Current @ 3.3 V	9	mA
Current @ 5 V	35	mA

Table 5: Power consumption

## 5 Environmental Conditions

### 5.1 Conditions

Condition	Min	Max
Operating Temperature [°C]	-40	+85
Storage Temperature [°C]	-40	+105
Relative humidity [%]	5	95

Table 6: Operating conditions

### 5.2 Usage

Condition	Parameter
Usage	indoor
Pullution degree	2
Operating altitude	up to 2000m

Table 7: Operating usage

### 5.3 EMC and Environmental Compliance (Preliminary)

The standard version of the board is provided without formal EMC or safety certification.

The hardware design is developed with consideration of commonly applied IEC standards, including:

- **ESD immunity:** IEC 61000-4-2
- **Electrical fast transient (EFT/Burst):** IEC 61000-4-4
- **Surge immunity:** IEC 61000-4-5
- **Conducted RF immunity:** IEC 61000-4-6
- **Radiated RF immunity:** IEC 61000-4-3
- **EMC immunity (industrial):** IEC 61000-6-2
- **EMC emission (industrial):** IEC 61000-6-4
- **Safety / isolation reference:** IEC 62368-1

These standards are not verified for the standard product variant.

Compliance with specific standards, test levels, or safety requirements is not guaranteed unless explicitly specified.

If defined EMC or isolation requirements are provided, application-specific validation, testing, and certification can be supported. Upon request, product variants with validated performance, including labeling, certification, and test reports (e.g. Hi-Pot testing), can be delivered.

## 6 Delivery

The product is delivered as a partially assembled kit intended for final user assembly. Mechanical accessories and connector components required for standard evaluation and stacked operation are included.

Order Code	BE-IIS-HPP-T1L-REV.B
Condition	Assembly kit
Status	Partially assembled
Included Items	1× HAT 4× 15 mm spacers 1× 2×20 pin stackable header 2x Jumoer
REACH & RoHS	Compliant with EU Directive 2011/65/EU and REACH Regulation (EC) No 1907/2006

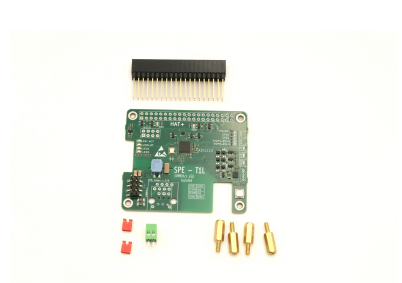


Figure 5: Delivery condition

## 7 Mechanical

### 7.1 Board Format

- Form factor: Raspberry Pi HAT+
- Mechanical dimensions: Raspberry Pi HAT compatible [5]
- Mounting hole pattern: Raspberry Pi HAT compatible [5]
- Stackszize: 15mm

### 7.2 Connectors and Assembly Height

- Host connector: 40-pin Raspberry Pi header
- Field connector: J6000, updated connector option
- Assembly height: [TODO]

### 7.3 Board Views

Figure 6: Mechanical overview

## 8 Assembly

This product is delivered as a kit and requires basic soldering and mechanical assembly.

### 8.1 2x20-Pin Main Connector

The 2x20-pin connector provides the interface to the Raspberry Pi. For proper HAT functionality, the connector must be assembled carefully.

A stackable 2x20-pin header is included in the delivery and is recommended for most applications, especially when using the BE-IIS HAT++ stacking system.

- Mount the header on the top side of the PCB (component side)
- The socket side faces down towards the Raspberry Pi

Alternatively, a standard (non-stackable) pin header may be used if stacking is not required.

#### **Soldering instructions:**

- Use a suitable soldering iron with adequate temperature control
- Ensure good ventilation and avoid inhaling solder fumes
- Heat both the pad and the pin simultaneously, then apply solder
- Solder each pin individually and ensure proper wetting
- Avoid excessive solder to prevent large solder cones, which may affect stacking capability

Proper alignment of the connector is important to ensure mechanical compatibility with the Raspberry Pi and other HATs.

## **8.2 Spacer**

To ensure mechanical stability and correct stacking height, spacers must be installed.

- Recommended spacer height: 15 mm
- Fix the PCB using appropriate screws and spacers
- Ensure stable mechanical mounting to avoid stress on the connector

The spacers define the stacking distance and provide mechanical fixation of the HAT.

## **8.3 3.5 mm Terminal Block Connector**

A suitable screw terminal block is typically included in the delivery. Alternatively, a compatible PCB header (plug or socket variant) may be used, depending on the application. Refer to the corresponding product section for supported connector types.

#### **Assembly instructions:**

- Ensure correct orientation before soldering: the cable entry openings must face outwards from the PCB edge
- Insert the connector fully into the PCB to ensure proper mechanical alignment
- Solder all pins carefully with sufficient wetting

#### **Important notes:**

- Avoid direct contact between the soldering iron and the plastic housing of the connector, as this may cause visible damage or deformation
- Ensure clean solder joints without excessive solder to maintain proper mechanical fit

Correct assembly ensures reliable electrical contact and proper usability of the terminal interface.

## 8.4 Board Overview

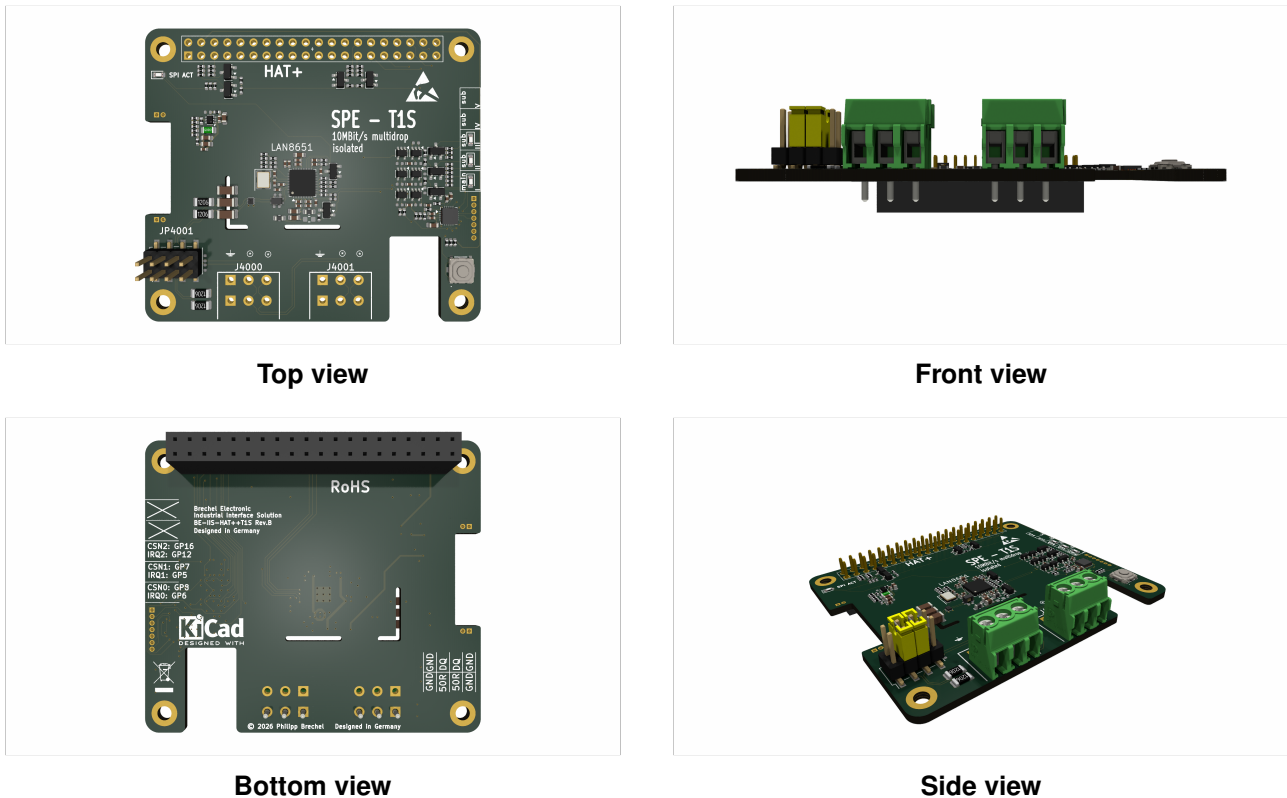


Figure 7: BE-IIS-HAT++T1S – mechanical overview

## 9 References

1. Microchip LAN8651 product page
2. BE-IIS Installer (Software and Setup Tools)
3. PhoenixContact PT 1,5/ 3-3,5-H - PCB terminal block
4. PhoenixContact MC 1,5/ 3-G-3,5 - PCB header
5. Raspberry Pi HAT+ Specification
6. [TODO: PCB layout and assembly documentation]

## 10 Revision History

Revision	Date	Description
A.00	2026-02-12	Initial draft
A.01	2026-02-12	Electrical and connector data added
A.02	2026-02-12	Content migrated from earlier draft