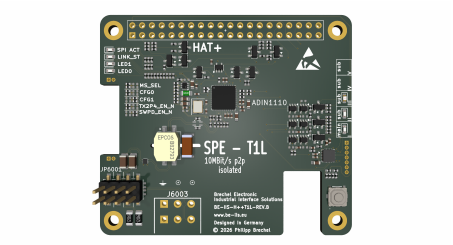
# 10BaseT1L Industrial HAT++

Brechel Electronic
Industrial Interface Systems
Designed by Philipp Brechel (Germany)
www.be-iis.eu | www.github.com/be-iis

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## 10BASE-T1L (IEEE 802.3cg) enables 10 Mbit/s Ethernet communication over a single twisted pair for long-reach point-to-point links.

### This HAT enables 10BASE-T1L communication based on an onboard Ethernet MAC-PHY.

## Key Features

- 10BASE-T1L compliant with IEEE 802.3cg
- ADIN1110 10BASE-T1L MAC-PHY
- Galvanically separated MDI
- Raspberry Pi HAT+ compliant (2024)
- Stackable HAT (BE-IIS-HAT++)
- Configurable CS and IRQ routing
- Optional PoSPE support
- Connector J6000 updated to new connector option
- RoHS compliant
- Quality component suppliers

## Product Description

The 10BASE-T1L Industrial Ethernet HAT is a Raspberry Pi HAT+ compliant Single Pair Ethernet interface board in accordance with IEEE 802.3cg. It integrates an ADIN1110 10BASE-T1L MAC-PHY and provides galvanic separation between the logic side and the field-side interface.

## Applications

- Technology evaluation
- Industrial network evaluation
- Prototyping
- Education and laboratory use
- Long-reach Ethernet node evaluation

## Contents

# 1 Introduction

The BE-IIS HAT++ 10BASE-T1L Industrial HAT is a Raspberry Pi HAT+ compliant interface board for 10BASE-T1L communication in industrial and laboratory environments.

The board integrates an ADIN1110 10BASE-T1L MAC-PHY [1]. The MDI is galvanically separated from the logic domain.

The HAT supports 10BASE-T1L operation and can be used for evaluation, prototyping, industrial network testing, and educational purposes.

Optionally, an add-on HAT is available to provide Power over Single Pair Ethernet (PoSPE) [TODO].

The HAT is compatible with the Raspberry Pi Foundation HAT+ specification as well as the BE-IIS HAT++ system for advanced functionality such as stacking.

# 2 Hardware Configuration

## 2.1 Main Features

The BE-IIS-HAT++T1L enables 10BASE-T1L communication on Raspberry Pi platforms. It allows a standard Raspberry Pi platform (e.g. Raspberry Pi Zero or Raspberry Pi 3/4/5, excluding Compute Module variants) to operate as a 10BASE-T1L node. Communication between the Raspberry Pi and the onboard MAC-PHY is implemented via the SPI interface with an interrupt line for event handling.

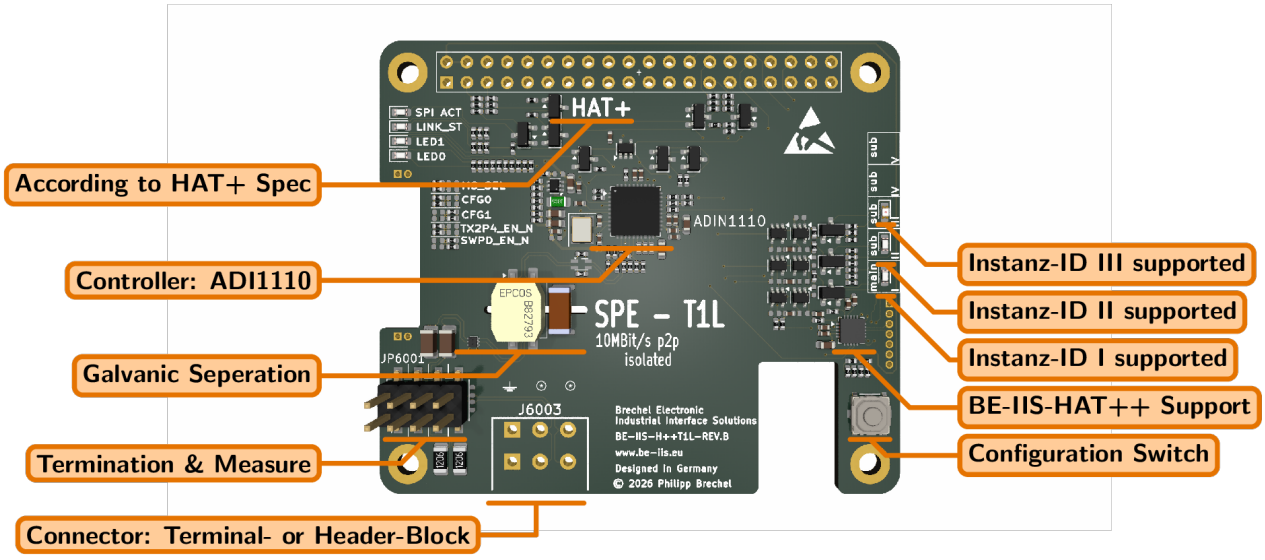



Figure 1: BE-IIS 10BASE-T1L top view with annotations

### MAC-PHY

- Supplier: Analog Devices
- ADIN1110 10BASE-T1L MAC-PHY
- Crystal 25MHz

### SPI Interface

- SPI0.0, SPI0.1, and SPI0.2 supported
- Persistent selection via push button

### Isolation

- Galvanically separated MDI
- Implemented by transformer coupling
- Transformer dielectric test rating: 2250 V DC / 60 s

### Power over Dataline

- Combination with a PoSPE HAT possible
- Supports currents up to 1 A
- Supports input voltages from 9 V to 33 V
- Includes an integrated 5 V main supply

### Protocol Support

- 10BASE-T1L according to IEEE 802.3cg

### Transmit Amplitude

- 1.0 $V_{p-p}$
- 2.4 $V_{p-p}$
- Controlled by autonegotiation

### Master / Slave

- Prefer Slave (default)
- Role determined by autonegotiation

### SPI Protocol

- Generic SPI
- 8-bit CRC

## 2.2 Block Diagram

The block diagram shown in Figure 2 is simplified. It illustrates the main functional blocks, power domains, separation barriers, and the principal data paths of the system.

The interrupt signal routing is not shown. It is configured using the same scheme as the chip-select (CS) routing. Reset and auxiliary control signals are omitted for clarity.

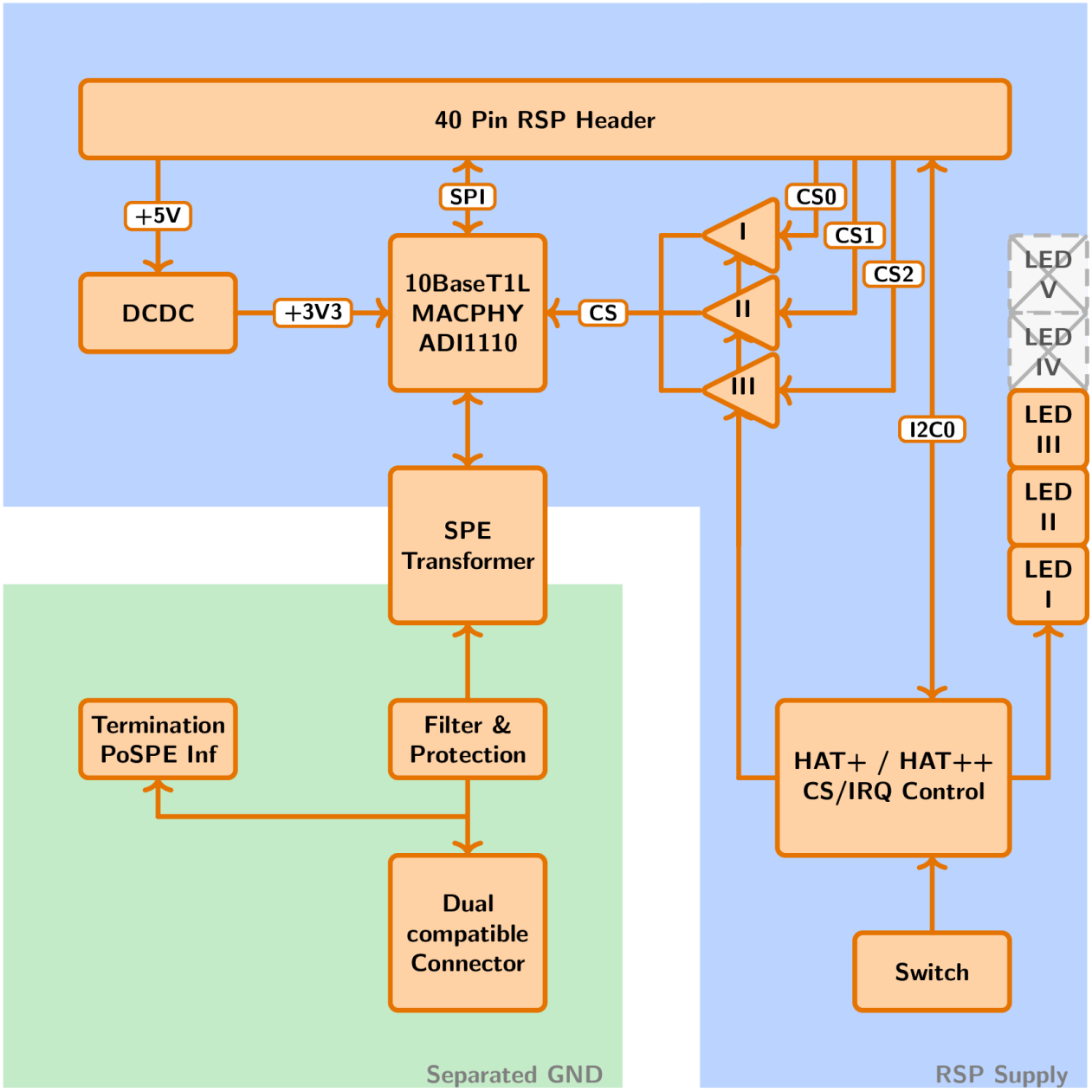



Figure 2: Simplified block diagram

## 2.3 HAT Configuration

The BE-IIS-HAT++ system is fully compliant with the Raspberry Pi HAT+ specification.

The HAT automatically provides its device tree overlay via the onboard EEPROM. As a result, no manual configuration through the bootloader or user-space tools is required. The device tree overlay defines the software configuration of the HAT hardware.

In addition, the BE-IIS-HAT++ system extends the standard HAT+ functionality by supporting multiple hardware configurations on a single HAT.

Up to three predefined configurations can be stored and selected. Each configuration is referred to as an **instance mode**. An instance mode defines the assignment and usage of interfaces such as SPI, $I^2C$, GPIO, and interrupt lines.

This enables:

- Operation of multiple identical HATs within one system
- Combination of several BE-IIS-HAT++ modules
- Flexible interface mapping without manual reconfiguration

## 2.4 Instance Modes and System Constraints

Instance Mode I corresponds to the primary Raspberry Pi HAT+ configuration. A HAT operating in this mode enables the $I^2C$ pull-ups and participates in the HAT+ EEPROM detection mechanism.

For proper system operation, exactly one HAT must be configured in Instance Mode I.

In stacked configurations:

- One HAT must operate in Instance Mode I
- Additional HATs must use alternative instance modes
- No two HATs may use the same instance mode simultaneously

The BE-IIS-HAT++ system supports stacking of up to five HATs, depending on the selected instance modes and system configuration.

## 2.5 Interfaces

The board interfaces with the host system via an SPI bus and a dedicated interrupt (IRQ) signal.

The SPI bus is used for communication between the Raspberry Pi (SPI master) and the onboard MAC-PHY (SPI slave). An interrupt line is used for event-driven communication.

The supported instance modes define the assignment of chip-select (CS) and interrupt (IRQ) signals:

| Instance Mode | CS | IRQ |
|---|---|---|
| I | GPIO8 | GPIO6 |
| II | GPIO7 | GPIO5 |
| III | GPIO16 | GPIO12 |

Table 1: Exclusive HW resources

| Instance Mode | Signal | Pin |
|---|---|---|
| I & II & III | SCLK | GP11 |
| I & II & III | MISO | GP9 |
| I & II & III | MOSI | GP10 |
| I & II & III | RESET | GP13 |
| I & II & III | SCL0 | GP1 |
| I & II & III | SDA0 | GP0 |

Table 2: Shared HW resources

The CS and IRQ signals are exclusively occupied by the HAT in each instance mode.

The SPI bus signals are shared across all instance modes. These signals may also be shared with additional HATs, provided that proper chip-select separation is ensured.

**HAT+ / HAT++ functionality**

The I²C bus **I2C0** (SDA0 / SCL0) is reserved for HAT identification and configuration purposes.

An onboard controller connected to I2C0 provides standard HAT+ identification data as well as extended HAT++ metadata. This includes, for example, device tree overlay references and configuration parameters used for automatic system integration.

The EEPROM content can be evaluated by the bootloader or by user-space software to dynamically apply device tree overlays and configure the system.

All other GPIO signals remain available for user applications, unless otherwise specified.

## 2.6 Isolation

Galvanic separation is implemented between the MDI signaling domain and the Raspberry Pi domain.

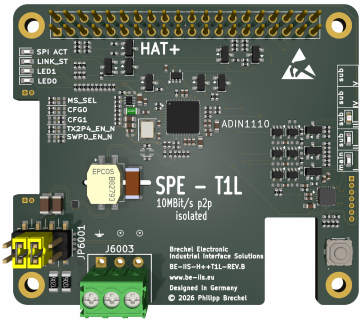
The separation barrier isolates the field-side interface from the logic-side circuitry, improving robustness against ground potential differences.

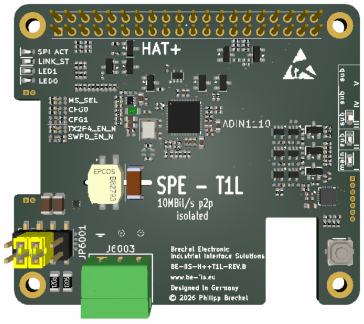
The separation is implemented using a transformer in the MDI path.

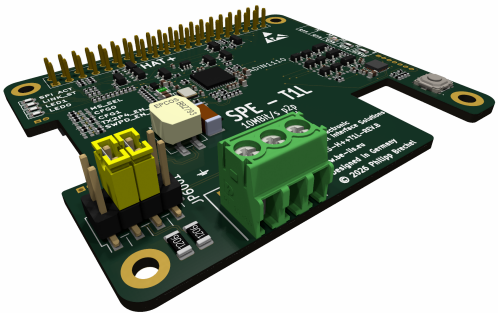
The isolation performance has not been formally validated. Users must evaluate the suitability of the separation concept for their specific application. Use of the isolation feature is at the user's own responsibility.

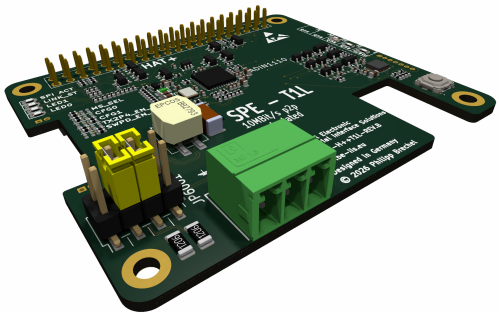
## 2.7 Connectors

Connectors J4000 and J4001 provides the physical MDI Bus interface. Both Connectors are placed on the same BUS for ease Multipdrop usage. Two commonly used connector options can be populated. on both connector lands





**Supplier:** Phoenix Contact
**MPN:** PT 1,5/3-3,5-H
**Order Code:** 1984620 [3]
**Description:** 3-pin 3.5 mm screw terminal block
**Note:** This connector is included in the delivery

**Supplier:** Phoenix Contact
**MPN:** MC 1,5/ 3-G-3,5 - PCB header
**Order Code:** 1844223 [4]
**Description:** 3-pin 3.5m mm PCB header

## 2.8 Jumper and Configuration

Jumper JP6001 provides configuration of the bus termination and, in combination with an optional PoSPE board, enables connection to the SPE signal line.
The jumper shall be installed by default. The intended use for removing the jumper is connection of a PoSPE board from the BE-IIS-HAT+ portfolio.
In 10BASE-T1L applications, termination is required in standard use cases.
Figure 3 shows the jumper configuration.

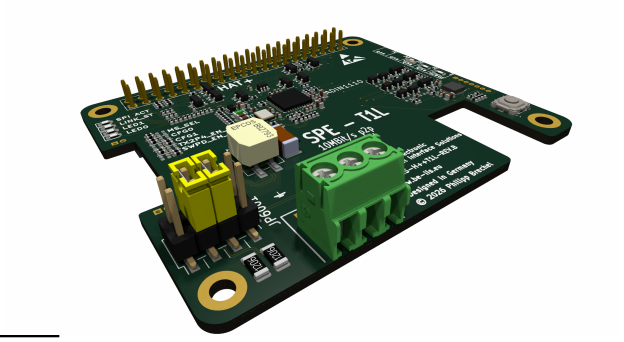



Figure 3: JP6001 jumper configuration

| Pin | Signal | Pin | Signal | Note |
|---|---|---|---|---|
| 1 | Shield | 2 | Shield | |
| 3 | Termination | 4 | SPE1 | Shorted by default |
| 5 | Termination | 6 | SPE2 | Shorted by default |
| 7 | Shield | 8 | Shield | |

Table 3: JP6001 pin assignment

## 2.9 Indicators (LEDs)

In addition to the LED status bar on the side, which indicates the selected instance mode, several indicator LEDs are placed on the HAT. Their functionality is described in Table 4.

| Reference | Name | Function | Default Behavior |
|---|---|---|---|
| D6004 | SPI ACT | SPI bus activity indicator | Active during SPI communication |
| D6003 | LINK_ST | Link status indicator | On when valid link is established |
| D6001 | LED1 | User-configurable LED | Disabled |
| D6002 | LED0 | User-configurable LED | On when valid link is established |

Table 4: LED functionality

## 2.10 Signal Polarity and Wiring Orientation

The two signal wires of the 10BASE-T1L interface are not polarity-sensitive. Either wire may be connected to either signal terminal.

Both wiring orientations are valid and supported by the interface.

This applies to normal data communication as well as to operation with power over the data line [TODO].

## 3 Software and System Configuration

The BE-IIS-HAT++ system provides a unified platform for fast system integration.

- Predefined drivers and kernel modules
- Support for prebuilt modules and custom kernel builds
- Ready-to-use build and configuration scripts
- Centralized software repository [TODO]
- Typical setup time below a few minutes

After installation, the system can be used without further software modification.

# 4 Electrical Characteristics

## 4.1 Supply Voltage

| Parameter | Min | Typ | Max |
|---|---|---|---|
| 3.3 V Input [V] | 3.135 | 3.3 | 3.65 |
| 5 V Input [V] | 4.5 | 5 | 5.5 |

Table 5: Voltage supply

## 4.2 Current Consumption

| Parameter | Typ | Unit |
|---|---|---|
| Current @ 5 V | 25 | mA |
| Current @ 3.3 V | 5 | mA |

Table 6: Current consumption

# 5 Environmental Conditions

## 5.1 Conditions

| Condition | Min | Max |
|---|---|---|
| Operating Temperature [°C] | -40 | +85 |
| Storage Temperature [°C] | -40 | +105 |
| Relative humidity [%] | 5 | 95 |

Table 7: Operating conditions

## 5.2 Usage

| Condition | Parameter |
|---|---|
| Usage | indoor |
| Pollution degree | 2 |
| Operating altitude | up to 2000 m |

Table 8: Operating usage

## 5.3 EMC and Environmental Compliance (Preliminary)

The standard version of the board is provided without formal EMC or safety certification.

The hardware design is developed with consideration of commonly applied IEC standards, including:

- **ESD immunity:** IEC 61000-4-2
- **Electrical fast transient (EFT/Burst):** IEC 61000-4-4
- **Surge immunity:** IEC 61000-4-5
- **Conducted RF immunity:** IEC 61000-4-6
- **Radiated RF immunity:** IEC 61000-4-3
- **EMC immunity (industrial):** IEC 61000-6-2
- **EMC emission (industrial):** IEC 61000-6-4
- **Safety / isolation reference:** IEC 62368-1

These standards are not verified for the standard product variant.

Compliance with specific standards, test levels, or safety requirements is not guaranteed unless explicitly specified.

If defined EMC or isolation requirements are provided, application-specific validation, testing, and certification can be supported. Upon request, product variants with validated performance, including labeling, certification, and test reports (e.g. Hi-Pot testing), can be delivered.

# 6 Delivery

The product is delivered as a partially assembled kit intended for final user assembly. Mechanical accessories and connector components required for standard evaluation and stacked operation are included.

| Order Code | BE-IIS-HPP-T1L-REV.B |
|---|---|
| Condition | Assembly kit |
| Status | Partially assembled |
| Included Items | 1× HAT<br>4× 15 mm spacers<br>1× 2×20 pin stackable header<br>2x Jumoer |
| REACH & RoHS | Compliant with EU Directive 2011/65/EU and REACH Regulation (EC) No 1907/2006 |

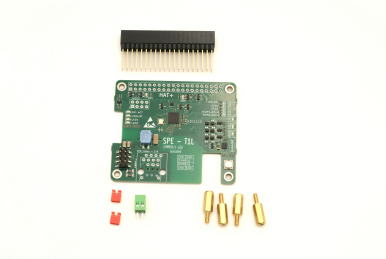


Figure 4: Delivery condition

# 7 Mechanical

## 7.1 Board Format

- Form factor: Raspberry Pi HAT+
- Mechanical dimensions: Raspberry Pi HAT compatible [5]
- Mounting hole pattern: Raspberry Pi HAT compatible [5]
- Stackszize: 15mm

## 7.2 Connectors and Assembly Height

- Host connector: 40-pin Raspberry Pi header
- Field connector: J6000, updated connector option
- Assembly height: [TODO]

## 7.3 Board Views

Figure 5: Mechanical overview

# 8 Assembly

This product is delivered as a kit and requires basic soldering and mechanical assembly.

## 8.1 2x20-Pin Main Connector

The 2x20-pin connector provides the interface to the Raspberry Pi. For proper HAT functionality, the connector must be assembled carefully.

A stackable 2x20-pin header is included in the delivery and is recommended for most applications, especially when using the BE-IIS HAT++ stacking system.

- Mount the header on the top side of the PCB (component side)
- The socket side faces down towards the Raspberry Pi

Alternatively, a standard (non-stackable) pin header may be used if stacking is not required.

**Soldering instructions:**

- Use a suitable soldering iron with adequate temperature control
- Ensure good ventilation and avoid inhaling solder fumes
- Heat both the pad and the pin simultaneously, then apply solder
- Solder each pin individually and ensure proper wetting
- Avoid excessive solder to prevent large solder cones, which may affect stacking capability

Proper alignment of the connector is important to ensure mechanical compatibility with the Raspberry Pi and other HATs.

### 8.2 Spacer

To ensure mechanical stability and correct stacking height, spacers must be installed.

- Recommended spacer height: 15 mm
- Fix the PCB using appropriate screws and spacers
- Ensure stable mechanical mounting to avoid stress on the connector

The spacers define the stacking distance and provide mechanical fixation of the HAT.

### 8.3 3.5 mm Terminal Block Connector

A suitable screw terminal block is typically included in the delivery. Alternatively, a compatible PCB header (plug or socket variant) may be used, depending on the application. Refer to the corresponding product section for supported connector types.

**Assembly instructions:**

- Ensure correct orientation before soldering: the cable entry openings must face outwards from the PCB edge
- Insert the connector fully into the PCB to ensure proper mechanical alignment
- Solder all pins carefully with sufficient wetting

**Important notes:**

- Avoid direct contact between the soldering iron and the plastic housing of the connector, as this may cause visible damage or deformation
- Ensure clean solder joints without excessive solder to maintain proper mechanical fit

Correct assembly ensures reliable electrical contact and proper usability of the terminal interface.

## 8.4 Board Overview

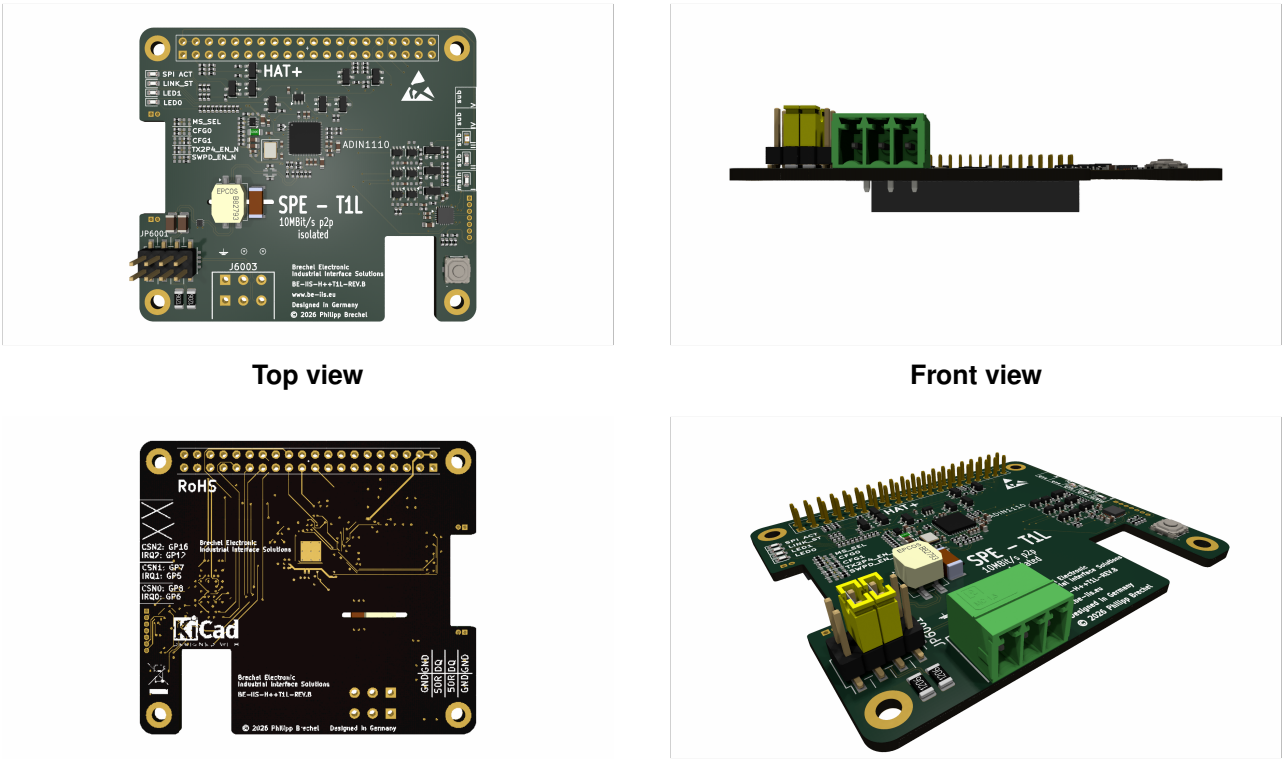



Figure 6: BE-IIS-HAT++T1L – mechanical overview

# 9 References

1. Analog Devices ADIN1110 product page
2. BE-IIS Installer (Software and Setup Tools)
3. PhoenixContact PT 1,5/ 3-3,5-H - PCB terminal block
4. PhoenixContact MC 1,5/ 3-G-3,5 - PCB header
5. Raspberry Pi HAT+ Specification
6. [TODO: PCB layout and assembly documentation]