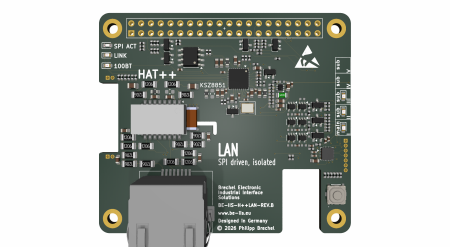
LAN Industrial HAT

Brechel Electronic
Industrial Interface Solutions
Designed by Philipp Brechel (Germany)
www.be-iis.eu | www.github.com/be-iis



Document ID: BE-IIS-HAT++LAN-DS
Revision: Rev. B
Date: April 2, 2026
Document Status: Draft
Product Status: Development

Standard Ethernet 10BASE-T / 100BASE-TX (10/100 Mbit/s) enables seamless integration into existing LAN infrastructures for industrial and embedded systems.

This HAT enables stackable LAN communication based on the KSZ8851 Ethernet controller, following the BE-IIS-HAT++ principle for seamless integration and simplified system expansion.

Key Features

- 10BASE-T / 100BASE-TX Ethernet, up to 100 Mbit/s
- KSZ8851 Ethernet controller (SPI)
- Integrated MAC + PHY
- RJ45 interface
- EEPROM for MAC-ADR
- RSP HAT+ compliant (2024)
- Stackable (BE-IIS-HAT++)
- Configurable CS & IRQ
- Auto-Negotiation support
- Compatible with standard LAN infrastructure
- RoHS compliant
- Quality component suppliers

Product Description

The Ethernet Industrial HAT is a Raspberry Pi HAT+ compliant interface board providing standard 10BASE-T / 100BASE-TX connectivity according to IEEE 802.3.
It integrates a KSZ8851SNLI-TR Ethernet controller with SPI interface, combining MAC and PHY in a single device for direct connection to standard LAN infrastructure.

Applications

- Ethernet / LAN network evaluation
- Debug Interfaces
- Embedded Ethernet prototyping
- Industrial network integration
- Gateway and protocol converter development
- Education and laboratory use

Contents

1 Introduction

The BE-IIS HAT++ Ethernet Industrial HAT is a Raspberry Pi HAT+ compliant interface board providing Ethernet connectivity for industrial and laboratory environments.

The board integrates a KSZ8851 SPI Ethernet controller [1], enabling a 10/100BASE-TX Ethernet interface via the SPI bus. The Ethernet interface is galvanically isolated from the logic domain.

The HAT can be used for evaluation, prototyping, industrial network integration, and educational purposes.

Optionally, the HAT can be combined with other BE-IIS HAT++ boards to extend functionality, such as additional communication interfaces or power supply modules.

The HAT is fully compatible with the Raspberry Pi Foundation HAT+ specification as well as the BE-IIS HAT++ system for advanced functionality such as stacking.

2 Hardware Configuration

2.1 Main Features

The BE-IIS-HAT++T1L enables 10BASE-T1L communication on Raspberry Pi platforms. It allows a standard Raspberry Pi platform (e.g. Raspberry Pi Zero or Raspberry Pi 3/4/5, excluding Compute Module variants) to operate as a 10BASE-T1L node. Communication between the Raspberry Pi and the onboard MAC-PHY is implemented via the SPI interface with an interrupt line for event handling.

2.2 Main Features

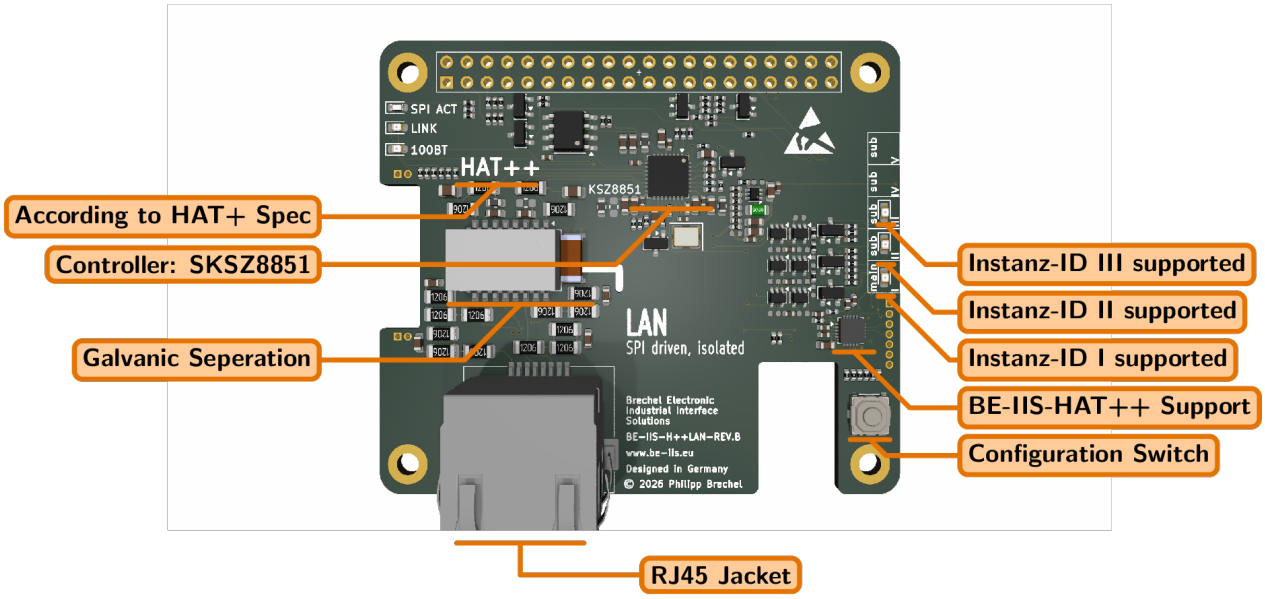


Figure 1: BE-IIS-LAN top view with annotations

Device

- Supplier: Microchip
- KSZ8851 10/100 Ethernet controller (MAC + PHY)
- Integrated MAC and PHY in single device (MACPhy)
- Mainline Linux kernel driver support

SPI Interface

- SPI0.0, SPI0.1, and SPI0.2 supported
- Persistent selection via push button

Isolation

- Galvanic decoupled MDI
- Performed by YAGEO isolation Transfomer
- Spezified up to 1500 V DC for 60 s
- EMI-robust differential signaling

Protocol Support

- IEEE 802.3 compliant (10BASE-T / 100BASE-TX)
- Auto-Negotiation suppor
- Hardware checksum offload (IP/TCP/UDP)
- Full- and Half-Duplex operation

Bus Topology

- Star topology using Ethernet switches
- Scalable node count depending on network infrastructure
- Long cable lengths up to 100 m

EEPROM populated

- MAC address storage
- Programmable via `ethtool`

2.3 Block Diagram

The block diagram shown in Figure 2 is simplified. It illustrates the power domains, isolation barriers, main functional blocks, and principal signal paths.

The interrupt signal routing is not shown. It is configured using the same scheme as the chip-select (CS) routing.

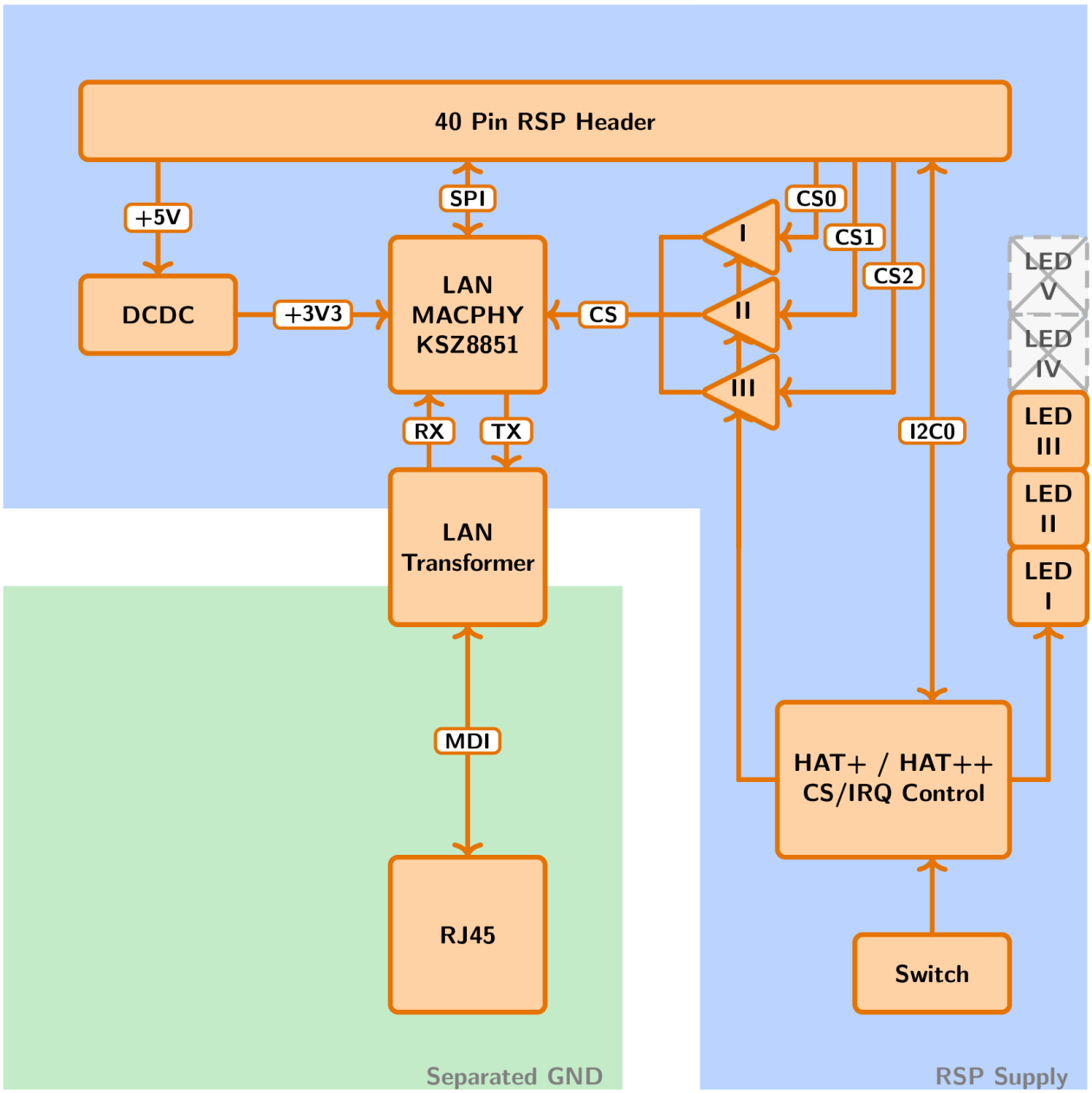


Figure 2: Simplified block diagram

2.4 HAT Configuration

The BE-IIS-HAT++ system is fully compliant with the Raspberry Pi HAT+ specification.

The HAT automatically provides its device tree overlay via the onboard EEPROM. As a result, no manual configuration through the bootloader or user-space tools is required. The device tree overlay defines the software configuration of the HAT hardware.

In addition, the BE-IIS-HAT++ system extends the standard HAT+ functionality by supporting multiple hardware configurations on a single HAT.

Up to three predefined configurations can be stored and selected. Each configuration is referred to as an **instance mode**. An instance mode defines the assignment and usage of interfaces such as SPI, I^2C, GPIO, and interrupt lines.

This enables:

- Operation of multiple identical HATs within one system
- Combination of several BE-IIS-HAT++ modules
- Flexible interface mapping without manual reconfiguration

2.5 Instance Modes and System Constraints

Instance Mode I corresponds to the primary Raspberry Pi HAT+ configuration. A HAT operating in this mode enables the I^2C pull-ups and participates in the HAT+ EEPROM detection mechanism.

For proper system operation, exactly one HAT must be configured in Instance Mode I.

In stacked configurations:

- One HAT must operate in Instance Mode I
- Additional HATs must use alternative instance modes
- No two HATs may use the same instance mode simultaneously

The BE-IIS-HAT++ system supports stacking of up to five HATs, depending on the selected instance modes and system configuration.

2.6 Interfaces

The board interfaces with the host system via an SPI bus and a dedicated interrupt (IRQ) signal.

The SPI bus is used for communication between the Raspberry Pi (SPI master) and the onboard MAC-PHY (SPI slave). An interrupt line is used for event-driven communication.

The supported instance modes define the assignment of chip-select (CS) and interrupt (IRQ) signals:

Instance Mode	CS	IRQ
I	GPIO8	GPIO6
II	GPIO7	GPIO5
III	GPIO16	GPIO12

Table 1: Exclusive HW resources

Instance Mode	Signal	Pin
I & II & III	SCLK	GP11
I & II & III	MISO	GP9
I & II & III	MOSI	GP10
I & II & III	RESET	GP13
I & II & III	SCL0	GP1
I & II & III	SDA0	GP0

Table 2: Shared HW resources

The CS and IRQ signals are exclusively occupied by the HAT in each instance mode.

The SPI bus signals are shared across all instance modes. These signals may also be shared with additional HATs, provided that proper chip-select separation is ensured.

HAT+ / HAT++ functionality

The I^2C bus **I2C0** (SDA0 / SCL0) is reserved for HAT identification and configuration purposes.

An onboard controller connected to I2C0 provides standard HAT+ identification data as well as extended HAT++ metadata. This includes, for example, device tree overlay references and configuration parameters used for automatic system integration.

The EEPROM content can be evaluated by the bootloader or by user-space software to dynamically apply device tree overlays and configure the system.

All other GPIO signals remain available for user applications, unless otherwise specified.

2.7 Isolation

Galvanic separation is implemented between the MDI signaling domain and the Raspberry Pi domain.

The separation barrier isolates the field-side interface from the logic-side circuitry, improving robustness against ground potential differences.

The separation is implemented using a transformer in the MDI path.

The isolation performance has not been formally validated. Users must evaluate the suitability of the separation concept for their specific application. Use of the isolation feature is at the user's own responsibility.

2.8 Connectors

A shielded RJ45 connector is used for the Ethernet interface. The connector is pre-assembled and soldered on the board.

2.9 Jumper and Configuration

The board does not provide any jumpers or user-accessible configuration options. All functionality is defined by the hardware design and controlled via software.

2.10 Indicators (LEDs)

The board provides visual status indication for both the SPI interface and the Ethernet link. These indicators support quick diagnostics during operation, installation, and troubleshooting.

- **CS-ACT**: Bus activity of SPI interface
  - *on*: SPI transaction ongoing
  - *off*: SPI bus idle
- **LED1 - Speed**: Link speed indication of Ethernet interface
  - *on*: 100BASE-TX
  - *off*: 10BASE-T
- **LED0 - Link**: Link and activity indication of Ethernet interface
  - *blinking*: Data activity

– *on*: Link established
– *off*: No link

The Ethernet-related LEDs are directly driven by the PHY and reflect the actual link status independently of software configuration.

2.11 Signal Polarity and Wiring Orientation

The Ethernet interface uses a standard RJ45 connector with integrated auto-negotiation and automatic MDI/MDI-X crossover detection.

The PHY automatically adapts to the cable wiring, allowing the use of both straight-through and crossover Ethernet cables without user intervention.

Any standard CAT5 (or higher) twisted-pair Ethernet cable can be used.

3 Software and System Configuration

The BE-IIS-HAT++ system provides a unified platform for fast system integration.

- Predefined drivers and kernel modules
- Support for prebuilt modules and custom kernel builds
- Ready-to-use build and configuration scripts
- Centralized software repository [TODO]
- Typical setup time below a few minutes

After installation, the system can be used without further software modification.

4 Electrical Characteristics

4.1 Supply Voltage

Parameter	Min	Typ	Max
3.3 V Input [V]	3.1	3.30	3.5
5 V Input [V]	4.5	5	5.5

Table 3: Voltage supply

4.2 Current Consumption

Parameter	Typ	Unit
Current @ 5 V	85	mA
Current @ 3.3 V	15	mA

Table 4: Current consumption

5 Environmental Conditions

5.1 Conditions

Condition	Min	Max
Operating Temperature [°C]	-40	+85
Storage Temperature [°C]	-40	+105
Relative humidity [%]	5	95

Table 5: Operating conditions

5.2 Usage

Condition	Parameter
Usage	indoor
Pollution degree	2
Operating altitude	up to 2000 m

Table 6: Operating usage

5.3 EMC and Environmental Compliance (Preliminary)

The standard version of the board is provided without formal EMC or safety certification.

The hardware design is developed with consideration of commonly applied IEC standards, including:

- **ESD immunity:** IEC 61000-4-2
- **Electrical fast transient (EFT/Burst):** IEC 61000-4-4
- **Surge immunity:** IEC 61000-4-5
- **Conducted RF immunity:** IEC 61000-4-6
- **Radiated RF immunity:** IEC 61000-4-3
- **EMC immunity (industrial):** IEC 61000-6-2
- **EMC emission (industrial):** IEC 61000-6-4
- **Safety / isolation reference:** IEC 62368-1

These standards are not verified for the standard product variant.

Compliance with specific standards, test levels, or safety requirements is not guaranteed unless explicitly specified.

If defined EMC or isolation requirements are provided, application-specific validation, testing, and certification can be supported. Upon request, product variants with validated performance, including labeling, certification, and test reports (e.g. Hi-Pot testing), can be delivered.

6 Delivery

The product is delivered as a partially assembled kit intended for final user assembly. Mechanical accessories and connector components required for standard evaluation and stacked operation are included.

Order Code	BE-IIS-HPP-LAN-REV.B
Condition	Assembly kit
Status	Partially assembled
Included Items	1× HAT 4× 15 mm spacers 1× 2×20 pin stackable header
REACH & RoHS	Compliant with EU Directive 2011/65/EU and REACH Regulation (EC) No 1907/2006

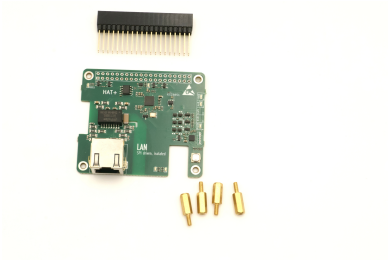


Figure 3: Delivery condition

7 Mechanical

7.1 Board Format

- Form factor: Raspberry Pi HAT+
- Mechanical dimensions: Raspberry Pi HAT compatible [3]
- Mounting hole pattern: Raspberry Pi HAT compatible [3]
- Stackszize: 15mm

7.2 Connectors and Assembly Height

- Host connector: 40-pin Raspberry Pi header
- Field connector: J6000, updated connector option
- Assembly height: [TODO]

7.3 Board Views

Figure 4: Mechanical overview

8 Assembly

This product is delivered as a kit and requires basic soldering and mechanical assembly.

8.1 2x20-Pin Main Connector

The 2x20-pin connector provides the interface to the Raspberry Pi. For proper HAT functionality, the connector must be assembled carefully.

A stackable 2x20-pin header is included in the delivery and is recommended for most applications, especially when using the BE-IIS HAT++ stacking system.

- Mount the header on the top side of the PCB (component side)
- The socket side faces down towards the Raspberry Pi

Alternatively, a standard (non-stackable) pin header may be used if stacking is not required.

Soldering instructions:

- Use a suitable soldering iron with adequate temperature control
- Ensure good ventilation and avoid inhaling solder fumes
- Heat both the pad and the pin simultaneously, then apply solder
- Solder each pin individually and ensure proper wetting
- Avoid excessive solder to prevent large solder cones, which may affect stacking capability

Proper alignment of the connector is important to ensure mechanical compatibility with the Raspberry Pi and other HATs.

8.2 Spacer

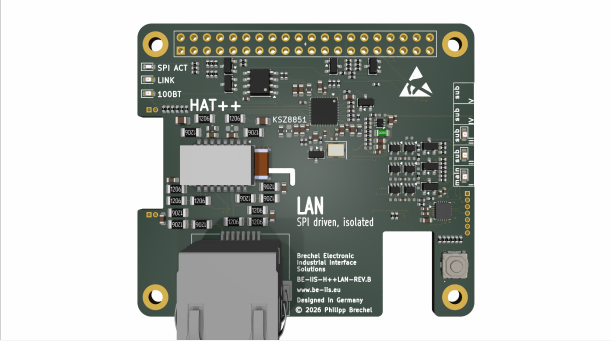
To ensure mechanical stability and correct stacking height, spacers must be installed.

- Recommended spacer height: 15 mm
- Fix the PCB using appropriate screws and spacers
- Ensure stable mechanical mounting to avoid stress on the connector

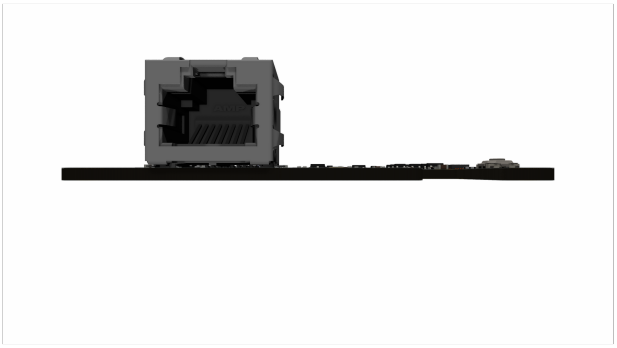
The spacers define the stacking distance and provide mechanical fixation of the HAT.

8.3 Board Overview

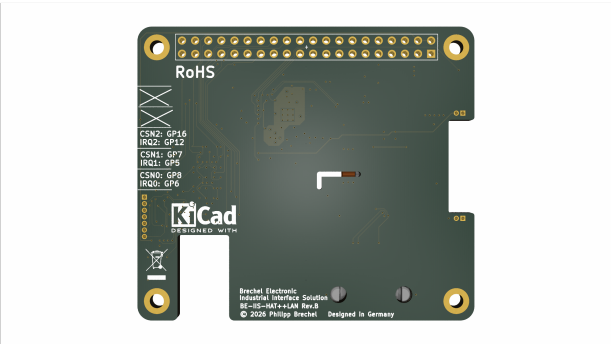
9 References



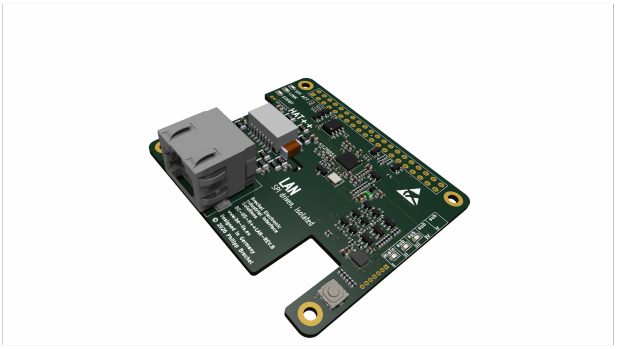
Top view



Front view



Bottom view



Side view

Figure 5: BE-IIS-HAT++ LAN – mechanical overview

1. KSZ8851 Product Webside
2. BE-IIS Installer (Software and Setup Tools)
3. Raspberry Pi HAT+ Specification
4. [TODO: PCB layout and assembly documentation]